**Lab 1: Logic Gates**

**ITI 1100 C – Digital Systems 1**

**Winter 2016**

**School of Electrical Engineering and Computer Science**

**University of Ottawa**

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Experiment Date: 2016-02-02

Submission Date: 2016-02-23

**Lab 1: Logic Gates**

**Objectives**

* Construct simple combinational logic circuits from a schematic
* Experimentally determine the functional operation of simple combinational logic circuits
* Identify common logic functions produced by various circuit configurations by the resulting truth table
* Connect various gates together to create simple logic functions
* Analyze combinational logic circuits and predict their operation
* Construct and test more complex combinational logic circuits

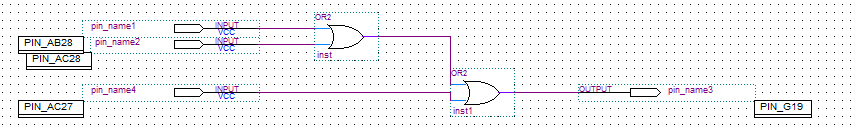
**Equipment and Components**

* Quartus II 13.0 Service-Pack 1 Software (64-bit)
* Altera DE2-115 circuit board
* Altera DE2-115 chip (EP4CE115F29C7N)
* Wire strippers

**Circuit Diagrams**

**Part 1 – Combinational Logic Circuits Construction**

**Figure 5.1.1:** One Chip Logic Circuit



R

B

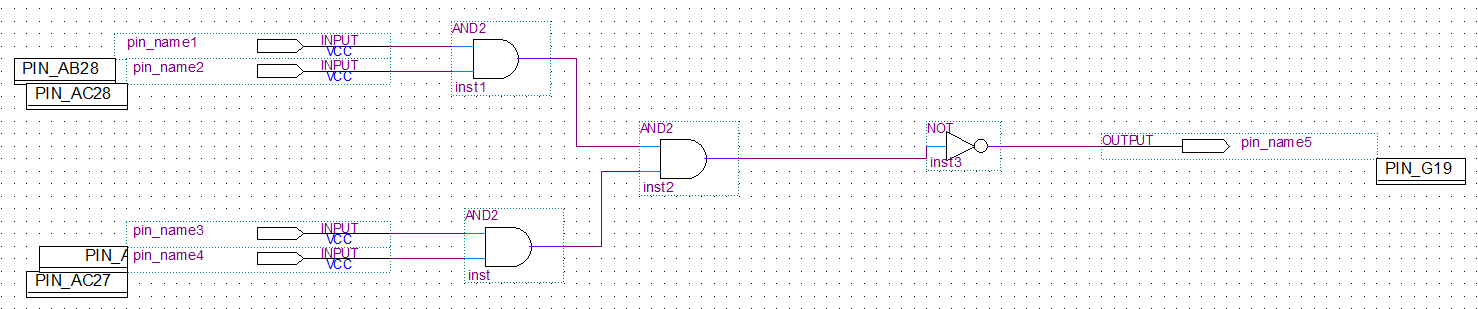
C

A

Inputs: A, B, C

Output: R

**Figure 5.1.2:** Two-Chip Logic Circuit



D

B

C

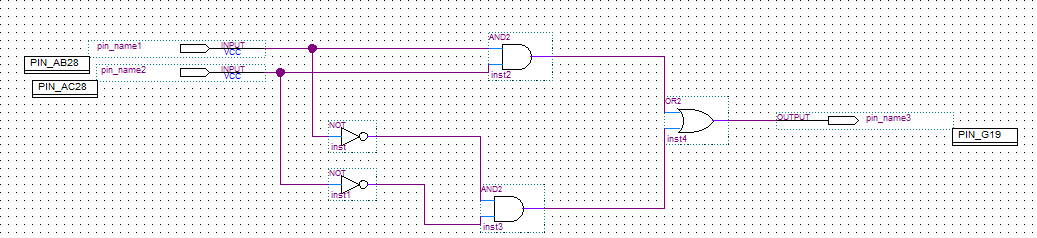
A

U

Inputs: A, B, C, D

Output: U

**Figure 5.1.3:** Three-Chip Logic Circuit



K

B

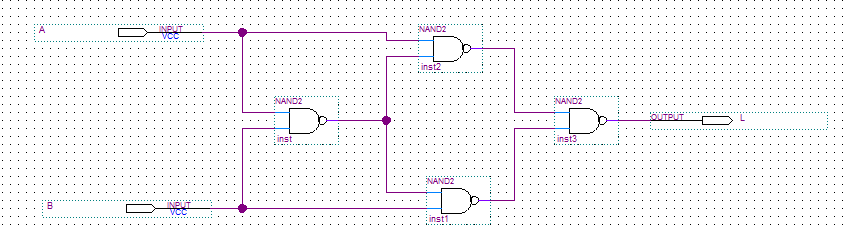
A

Inputs: A, B

Output: K

**Part II - Combinational Logic Circuits Analysis**

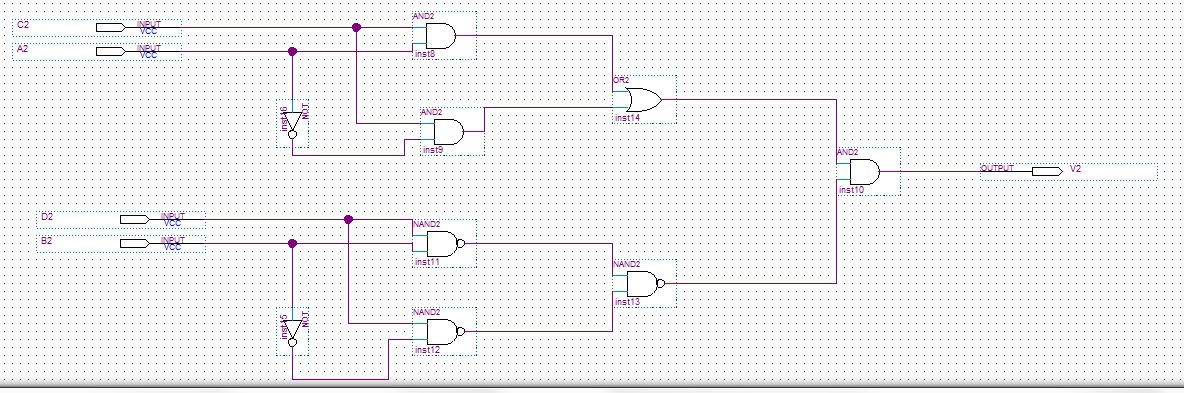
**Figure 5.1.5:** Exclusive OR Circuit



Inputs: A, B

Output: L

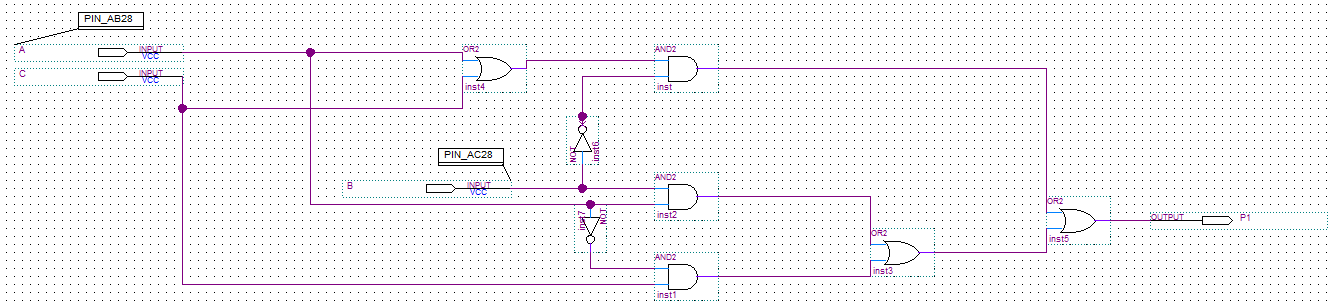
**Figure 5.1.6:** AND Circuit



Inputs: A2, B2, C2, D2

Output: V2

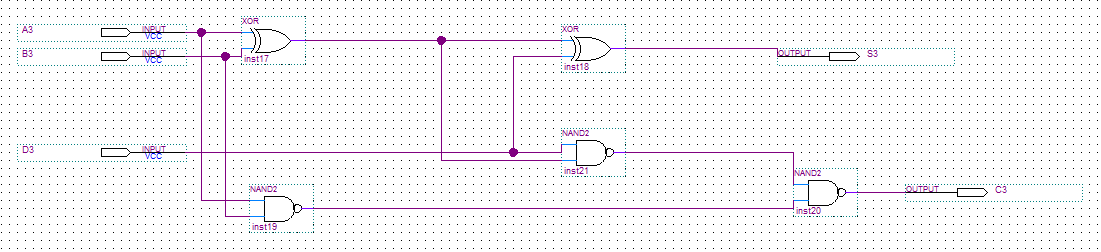
**Figure 5.1.7:** OR Circuit



Inputs: A, B, C

Output: P1

**Figure 5.1.8:** Multiple Output Circuit



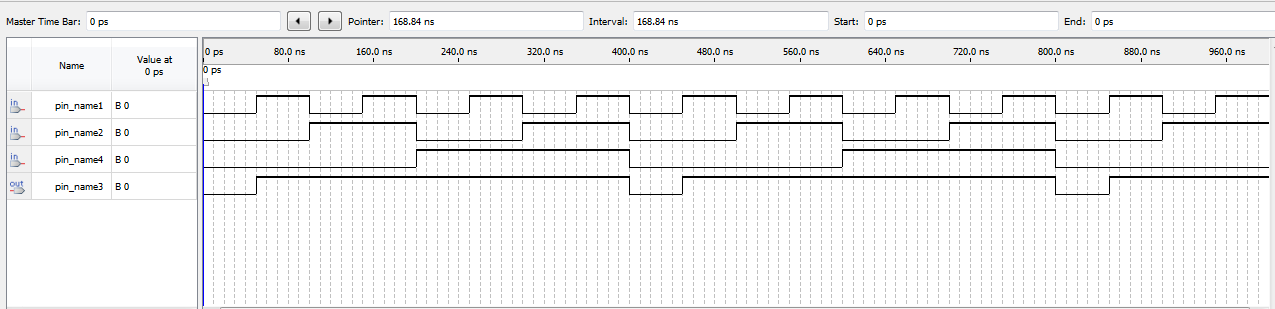
Inputs: A3, B3, D3

Outputs: S3, C3

**Experimental Data and Data Processing**

**Part 1 – Combinational Logic Circuits Construction**

**Figure 5.1.1:** One-Chip Logic Circuit



C

A

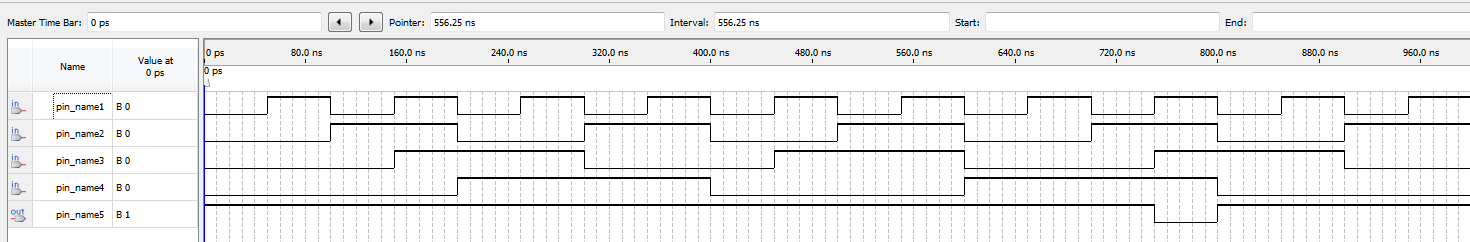
B

R

**Table 1:** Experimental Data Observed from Circuit 5.1.1

|  |  |  |  |
| --- | --- | --- | --- |
| **Input Given** | | | **Observed Output** |
| **A** | **B** | **C** | **R** |
| 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 |

**Figure 5.1.2:** Two-Chip Logic Circuit



B

A

C

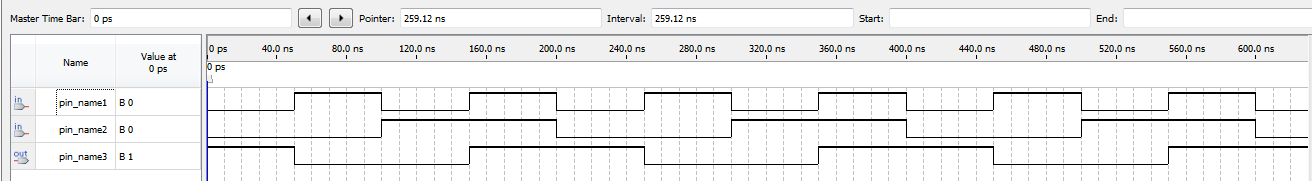
D

U

**Table 2:** Experimental Data Observed from Circuit 5.1.2

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Input Given** | | | | **Observed Output** |
| **A** | **B** | **C** | **D** | **U** |
| 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 |

**Figure 5.1.3:** Three-Chip Logic Circuit



B

A

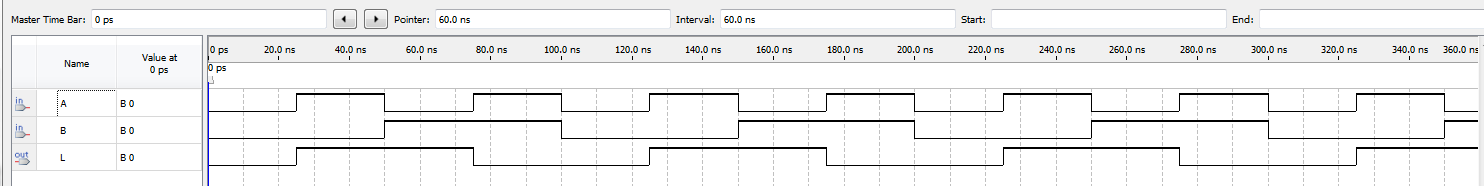
K

**Table 3:** Experimental Data Observed from Circuit 5.1.3

|  |  |  |
| --- | --- | --- |
| **Input Given** | | **Observed Output** |
| **A** | **B** | **K** |
| 1 | 1 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 0 | 0 | 1 |

**Part II - Combinational Logic Circuits Analysis**

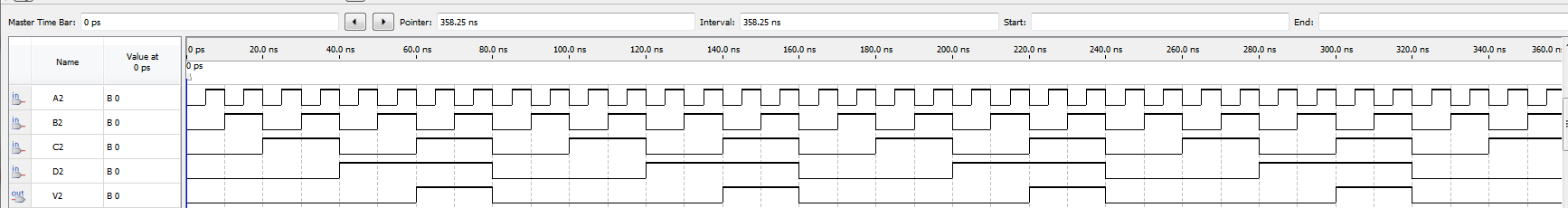
**Figure 5.1.5:** Exclusive OR Circuit



**Table 4:** Experimental Data Observed from Circuit 5.1.5

|  |  |  |
| --- | --- | --- |
| **Input Given** | | **Observed Output** |
| **A** | **B** | **L** |
| 1 | 1 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 0 | 0 | 0 |

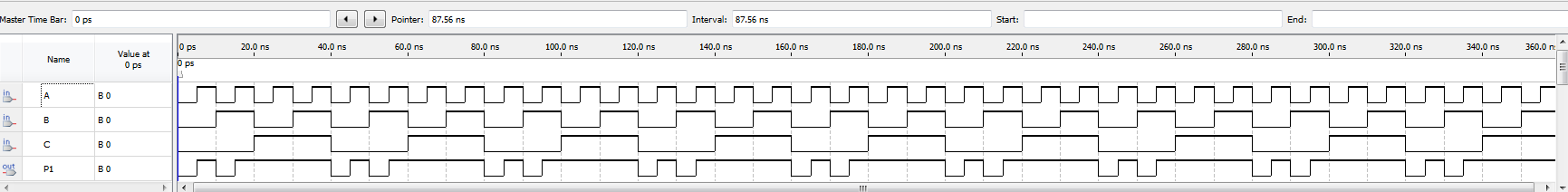
**Figure 5.1.6:** AND Circuit



**Table 5:** Experimental Data Observed from Circuit 5.1.6

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Input Given** | | | | **Observed Output** |
| **A2** | **B2** | **C2** | **D2** | **V2** |
| 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 |

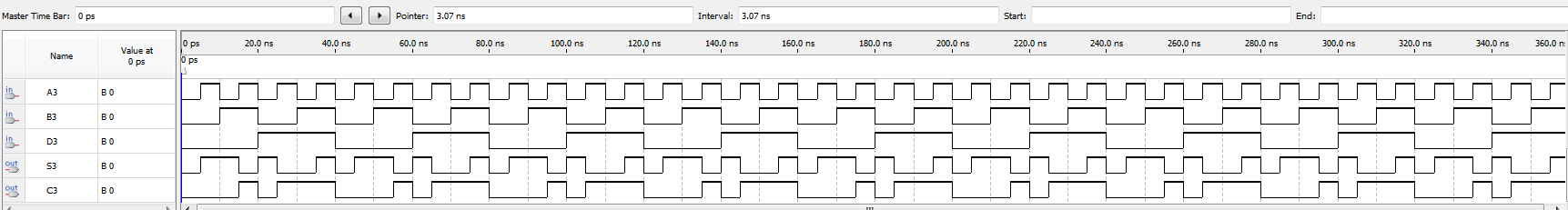
**Figure 5.1.7:** OR Circuit



**Table 6:** Experimental Data Observed from Circuit 5.1.7

|  |  |  |  |
| --- | --- | --- | --- |
| **Input Given** | | | **Observed Output** |
| **A** | **B** | **C** | **P1** |
| 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 |

**Figure 5.1.8:** Multiple Output Circuit



**Table 7:** Experimental Data Observed from Circuit 5.1.8

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Input Given** | | | **Observed Output** | |
| **A3** | **B3** | **D3** | **S3** | **C3** |
| 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 |

**Comparison of Theoretical Data and Experimental Data**

**Part 1 – Combinational Logic Circuits Construction**

**Table 8:** Comparison of Theoretical and Experimental Results of Circuit 5.1.1

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Input Given** | | | **Observed Results** | **Expected Results** |
| **A** | **B** | **C** | **R** | **R** |
| 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 |

The result observed experimentally for the One-Chip Circuit were identical to the results obtained theoretically as expected due to the laws of Boolean logic.

**Table 9:** Comparison of Theoretical and Experimental Results of Circuit 5.1.2

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Input Given** | | | | **Observed Results** | **Expected Results** |
| **A** | **B** | **C** | **D** | **U** | **U** |
| 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 |

The result observed experimentally for the Two-Chip Circuit were identical to the results obtained theoretically as expected due to the laws of Boolean logic.

**Table 10:** Comparison of Theoretical and Experimental Results of Circuit 5.1.3

|  |  |  |  |
| --- | --- | --- | --- |
| **Input Given** | | **Observed Results** | **Expected Results** |
| **A** | **B** | **K** | **K** |
| 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 |

The result observed experimentally for the Three-Chip Circuit were identical to the results obtained theoretically as expected due to the laws of Boolean logic.

**Part II - Combinational Logic Circuits Analysis**

**Table 11:** Comparison of Theoretical and Experimental Results of Circuit 5.1.5

|  |  |  |  |
| --- | --- | --- | --- |
| **Input Given** | | **Observed Results** | **Expected Results** |
| **A** | **B** | **L** | **L** |
| 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 |

The result observed experimentally for the Exclusive-OR Circuit were identical to the results obtained theoretically as expected due to the laws of Boolean logic.

**Table 12:** Comparison of Theoretical and Experimental Results of Circuit 5.1.6

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Input Given** | | | | **Observed Results** | **Expected Results** |
| **A2** | **B2** | **C2** | **D2** | **V2** | **V2** |
| 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 |

The result observed experimentally for the AND Circuit were identical to the results obtained theoretically as expected due to the laws of Boolean logic.

**Table 13:** Comparison of Theoretical and Experimental Results of Circuit 5.1.7

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Input Given** | | | **Observed Results** | **Expected Results** |
| **A** | **B** | **C** | **P1** | **P1** |
| 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 |

The result observed experimentally for the OR Circuit were identical to the results obtained theoretically as expected due to the laws of Boolean logic.

**Table 14:** Comparison of Theoretical and Experimental Results of Circuit 5.1.8

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Input Given** | | | **Observed Results** | | **Expected Results** | |
| **A3** | **B3** | **D3** | **S3** | **C3** | **S3** | **C3** |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The result observed experimentally for the Multiple Output Circuit were identical to the results obtained theoretically as expected due to the laws of Boolean logic.

**Discussion and Conclusions**

The objective of this experiment was to construct simple combinational logic circuits from a schematic, experimentally determine the functional operation, and analyze and predict their operations. We first predict the outcome theoretically by determining the output for every possible input combination. Then experimentally determine if our theoretical predictions are correct. Through the lab we notice that complicated circuits can sometimes be simplified and still have the same inputs and outputs. In the lab it was observed that the theoretical and actual inputs and outputs matched. This confirms the De Morgan’s Law which states complementing ports of an AND gate converts it to an OR gate and vice versa, complementing both ports of an inverter however leaves the operation unchanged. Since the theoretical and experimental results matched, the corresponding truth tables to the circuits were proved to be true.

**Appendix (Pre-Lab)**

See the next page for the truth table predictions written for the lab.